

Docket No. 243333US2S/phh

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Nobutaka KITAGAWA

SERIAL NO: 10/671,585

GAU:

FILED: September 29, 2003

EXAMINER:

FOR: ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Marvin J. Spivak

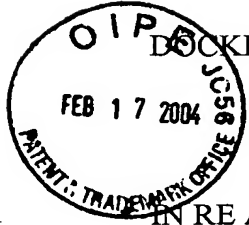
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STATEMENT OF RELEVANCY

Reference AO (JP 8-321586) on Form 1449:

This patent is about the common discharge line which is different from the Power/GND. As for the common trigger line, it is not specifying.

Reference AP (JP 6-5705) on form 1449:

This patent is about the common discharge line which is most large circuit GND. As for the common trigger line, it is not specifying.

Reference AW on Form 1449:

This paper shows the way to having SCR dynamically control during ESD zapping. However, a trigger point is not used for the control of the other protection circuit.



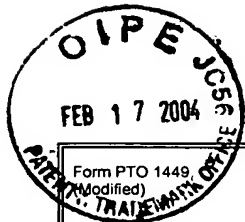
LIST OF RELATED CASES

<u>Docket Number</u>	<u>Serial or Patent Number</u>	<u>Filing or Issue Date</u>	<u>Inventor/ Applicant</u>
236680US2S	10/417,112	04/17/03	KITAGAWA
243333US2S*	10/671,585	09/29/03	KITAGAWA

*Present Application; listed for information

EHK/sb

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Form PTO 1449
(Modified)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY DOCKET NO.

243333US2S

SERIAL NO.

10/671,585

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT

Nobutaka KITAGAWA

FILING DATE

September 29, 2003

GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	5,821,804	10/13/1998	W. NIKUTTA, et al.			
	AB	5,079,612	01/07/1992	H. TAKAMOTO, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AO	8-321586	12/03/1996	JAPAN (with corr. US 5,821,804)		X
	AP	6-5705	01/19/1994	JAPAN (with corr. US 5,079,612)		X
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	M.-D. KER, et al., IEEE Journal of Solid-State Circuits, vol. 32, no. 1, pages 38-51, "A GATE-COUPLED PTLSCR/NTLSCR ESD PROTECTION CIRCUIT FOR DEEP-SUBMICRON LOW-VOLTAGE CMOS IC'S ", January 1997
	AX	
	AY	
	AZ	

☐ Additional References sheet(s) attached

Examiner

Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.